REMARKS

Claims 1-10 are currently pending in the subject application and subject to examination. Applicant wishes to thank the Examiner for the acknowledgement of allowable subject matter in claims 3, 5, 7 and 9.

Reconsideration of this application is respectfully requested in view of the following remarks.

Claims 1-10 Recite Patentable Subject Matter

Claims 1, 2, 6, 8 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No.: 5,337,050 to Sugawara (hereinafter, "Sugawara"). Claims 3-5, 7 and 9 are objected to as being dependent upon a rejection base claim, but would allowable if rewritten to include the limitations of the base claim and any intervening claims. Applicant respectfully traverses the rejection and objection, as follows.

Independent claims 1, 8 and 10 are directed to a data input circuit, a semiconductor device including a data input circuit and a method, respectively, for converting input serial data to n-bit parallel data and outputting the n-bit parallel data by following an address signal. The data input circuit of claims 1 and 8 includes, among other features, the features of a data shifting unit including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns, and a selection unit selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to said data shifting unit through the input column. Claim 10 includes, among other features, the features of selecting a column among a plurality of columns of a data shifting unit as an input column by following the address signal, inputting

the input serial data to said data shifting unit through the input column, and shifting the input serial data sequentially through the plurality of columns.

Sugawara discloses plural register blocks, each having a flip-flop circuit that holds data therein and outputs the data therefrom, and a gate circuit that receives two selection signals as inputs, in order to select the flip-flop circuit. The plural register blocks are arranged in a matrix form, and data is held by the selected register block. The address data used to select the register block from the plurality of register blocks is generated by a serial clock received at a serial clock input terminal CK. Serial data is inputted in synchronization with a serial clock. The data is held in the register block sequentially selected according to an address generated automatically by the clock. The data is outputted in a parallel manner at one time.

Unlike the data shifting unit in the claimed invention, the plural register blocks of Sugawara do not shift data from one register block to another register block. In contrast, in the claimed invention, in order to output n-bit parallel data from input serial data, the input serial data is shifted sequentially through the plurality of columns.

Furthermore, in Sugawara, the register block in which data is to be held is selected by the address generated automatically by the clock. To the contrary, in the present invention, an input column is selected according to the address signal supplied from the outside of the input circuit (the address signal is generated in accordance with a command signal supplied to the input circuit).

Thus, in Sugawara, the register block in which data is to be held is selected one after another according to the address generated automatically by the clock, whereas in the claimed invention, the plurality of columns forming the data shifting unit (i.e. a shift

register), and the input column through which the input serial data is inputted to the data shifting unit is determined according to the external address signal (the data input point of the shift register is changed according to the external address signal).

Therefore, Applicant respectfully submits that Sugawara fails to disclose or suggest at least the features of a data shifting unit including a plurality of columns, and sequentially shifting the input serial data through the plurality of columns, and a selection unit selecting a column among the plurality of columns as an input column by following the address signal, wherein the input serial data is inputted to said data shifting unit through the input column, as recited in claims 1 and 8. Further, Applicant respectfully submits that Sugawara fails to disclose or suggest at least the features of selecting a column among a plurality of columns of a data shifting unit as an input column by following the address signal, inputting the input serial data to said data shifting unit through the input column, and shifting the input serial data sequentially through the plurality of columns, as recited in claim 10.

Rather, as stated above, Sugawara discloses plural register blocks in which data is to be held, which are selected by an address generated automatically by a clock. Thus, the register block in which data is to be held in Sugawara cannot be changed by, for example, a write command. Therefore, in order to apply a configuration in the reference to an application in which the address signal input simultaneously with a write command may alter the sequence of input data that is to be input in succession, such as a data input circuit used for a Double Data Rate SDRAM, the configuration in Sugawara requires a data switch unit such as data switch unit 130 disclosed in Fig. 1 of the present application. Such a data switch unit 130 has many elements and increases

a circuit area of the input circuit, as is pointed out in the "Description of the Related Art" in the present application.

To establish *prima facie* obviousness of a rejected claim, the applied art of record must teach or suggest each and every feature of a rejected claim. See M.P.E.P. §2143.03. As explained above, Sugawara fails to disclose or suggest each and every feature of independent claims 1, 8 and 10. Thus, Applicant respectfully submits that independent claims 1, 8 and 10 are neither anticipated nor rendered obvious by Sugawara. Accordingly, Applicant respectfully submits that independent claims 1, 8 and 10 are allowable over Sugawara.

Claims 2-7 and 9 depend from claims 1 and 8, respectively. Thus, it is respectfully submitted that claims 2-7 and 9 are allowable for the same reasons as claims 1 and 8, as well as for the additional subject matter recited therein.

In view of the above, withdrawal of the rejection of claims 1, 2, 6, 8 and 10 under 35 USC § 103(a), and the objection to claims 3-5, 7 and 9 are respectfully requested.

CONCLUSION

For at least the above reasons, claims 1-10 are believed to be in condition for allowance and a notice to such effect is respectfully requested. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referencing Client Matter No. 100353-00040.

Respectfully submitted,

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